PARASITIC EFFECTS INDUCED BY POWER STRIPS CURRENT SWITCHING IN FULL WAFER PACKAGE

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ABSTRACT

Parasitic effects induced by current switching in power lines for full wafer packages (monolithic or hybrid) are analyzed in the time domain. Theoretical results allow to give simple relations in order to easily predict :

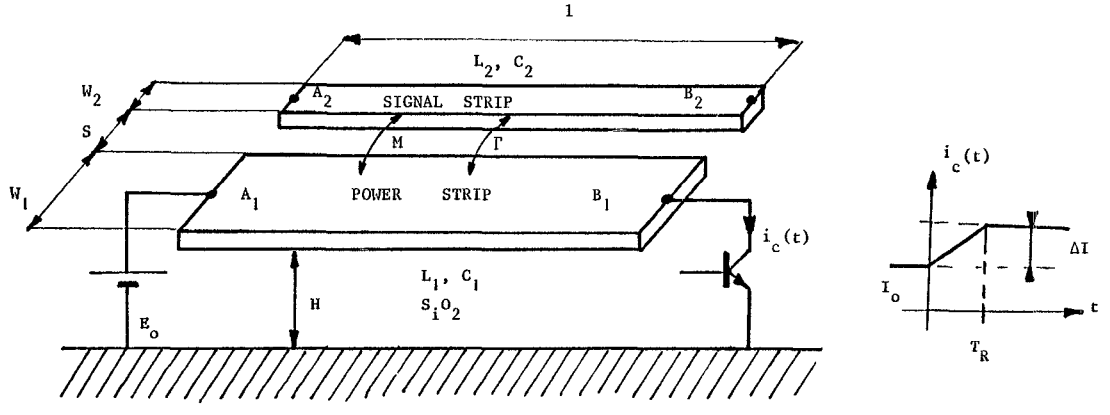
* the dynamic drop voltage on the power line,
* the parasitic voltages on signal lines, induced by coupling with power line.

Experimental measurements on typical devices validate these formula.

INTRODUCTION

Increasing progress obtained on silicon technology actually allows to process integrated circuits (IC) with very high complexity (more than 10^6 transistors) and high operating clock frequency (upper than 100 Mhz).

These kinds of IC need an increasing count of input/ouput pins (I/O) and also a very dense interconnection network . For saving their dynamic performances, these chips need to be mounted on sophisticated packages like S.C.C or M.C.C.; silicon wafers offer an attractive way to perform such pakages. In that case, only the interconnection network will be designed on the silicon substrate; it will be populated by hybridation with high performant IC's.



$W_1 \sim 50\ \mu m$ $S \sim 4\ \mu m$ $W_2 \sim 16\ \mu m$ $H \sim 3,5\ \mu m$

$l \sim 1\ cm$ $I_o \sim 1\ A$ $\Delta I \sim 0.1\ A$ $T_R \sim 500\ ps$

Figure 1

Typical device (silicon wafer package)

In such packages, parasitic effects induced by current switching in power lines might introduce dramatic limitation on operating clock frequency. The typical geometry of the two studied interconnection strips (power and signal lines) is given in figure 1.

THEORETICAL BACKGROUND

The primary electrical parameters of the lines are calculated following the method given in Ref. [1]; one obtains :

$$\begin{array}{llll} L_1 = & 70 \text{ pH/mm} & C_1 = & 596 \text{ fF/mm} \\ L_2 = & 162 \text{ pH/mm} & C_2 = & 245 \text{ fF/mm} \\ M = & 11{,}3 \text{ pH/mm} & \Gamma = & 28 \text{ fF/mm} \end{array} \quad (1)$$

The values of mutual coefficients M and Γ show that coupling between power and signal lines is weak. Using propagation concepts and taking into account mismatch effects at the two ends of the power line, theoretical analysis gives the relation between the dynamic drop voltage $v_{B1}(t)$ and the switching current $i_C(t)$ [2] :

$$v_{B1}(t) = \frac{R_{C1} \cdot R_{B1}}{R_{C1} + R_{B1}} \left(i_C(t) - 2 \sum_{n=1}^{\infty} (-\rho_{B1})^n \, i_C(t-2n\tau) \right) \quad (2)$$

where :

R_{C1} : characteristic impedance of the power line ($= \sqrt{L_1/C_1}$).

R_{B1} : equivalent resistance of the transistor ($= E_0/I_0$).

τ : round trip time on the power line ($= \sqrt{L_1/C_1}\, l$).

ρ_{B1} : reflexion coefficient at point $B_1 \left(= \frac{R_{B1} - R_{C1}}{R_{B1} + R_{C1}} \right)$

TIME DOMAIN ANALYSIS

In the case of "on chip" lines, the driving signal rise time T_R is usually much greater than the line round trip time τ . So the dynamic voltage $v_{B1}(t)$ reaches its maximum value ΔV_{B1} ; taking the limit of equation (2) (for $t \rightarrow \infty$), one obtains :

$$\Delta V_{B1} \# \frac{\tau}{T_R} R_{C1} \Delta I = L_1 l \frac{\Delta I}{T_R} \quad (3)$$

ΔI is the current swing in the power line. With ΔI = 100 mA the parasitic voltage ΔV_{B1} is about 140 mV. Figure 2 shows theoretical and experimental results obtained on the studied device in the subnano-second domain.

The mutual effects of a power line upon a signal line induce voltages at points A_2 and B_2 (forward and backward voltage). In the case of matched line, following [3] one obtains :

$$V_{A2}(t) \# \frac{k_{C2} - k_{L1}}{2} \tau \frac{\partial v_{B1}(t)}{\partial t}$$

$$V_{B2}(t) \# \frac{k_{C2} + k_{L1}}{2} \tau \frac{\partial v_{B1}(t)}{\partial t} \quad (4)$$

where : $k_{L1} = M/L_1$ and $k_{C2} = \Gamma/C_2$.

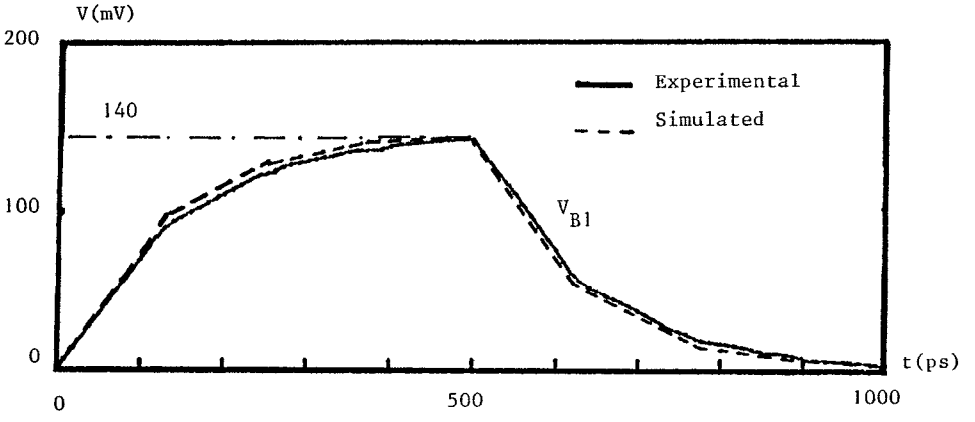


Figure 2

Dynamic drop voltage on power line due to a current switching

Actual signal line being unmatched, the induced voltages given in (4) are reflected at each end (open circuit). After an infinite summation, the voltages can be expressed under the closed form :

$$V_{A2}(t) \# \frac{k_{C2} - k_{L1}}{2} v_{B1}(t)$$

$$V_{B2}(t) \# \frac{k_{C2} + k_{L1}}{2} v_{B1}(t) \qquad (5)$$

Their maximal values are a function of the current swing on line 1; that is :

$$\Delta V_{A2} = \frac{k_{C2} - k_{L1}}{2} L_1 \, I \frac{\Delta I}{T_R}$$

$$\Delta V_{B2} = \frac{k_{C2} + k_{L1}}{2} L_1 \, I \frac{\Delta I}{T_R} \qquad (6)$$

In our case, $k_{L1} = 0,137$ and $k_{C2} = -0,023$; so we obtain $\Delta V_{A2} = -3$ mV and $\Delta V_{B2} = 19$ mV. Theoretical and experimental results obtained in the time domain are given in figure 3.

CONCLUSION

This analysis allows to develop optimization criteria for the full wafer interconnect layout or other advanced packages (Multi Chip Carrier).

The width W_1 governing the self inductance of the power line (L_1) must be kept as large as possible (in order to reduce ΔV_{B1}).

Coupling coefficients (k_{L1} and k_{C2}) are related to the spacing S between lines and the thickness H of the silicon oxide. In order to reduce ΔV_{A2} and ΔV_{B2}, S has to be increased, and H decreased.

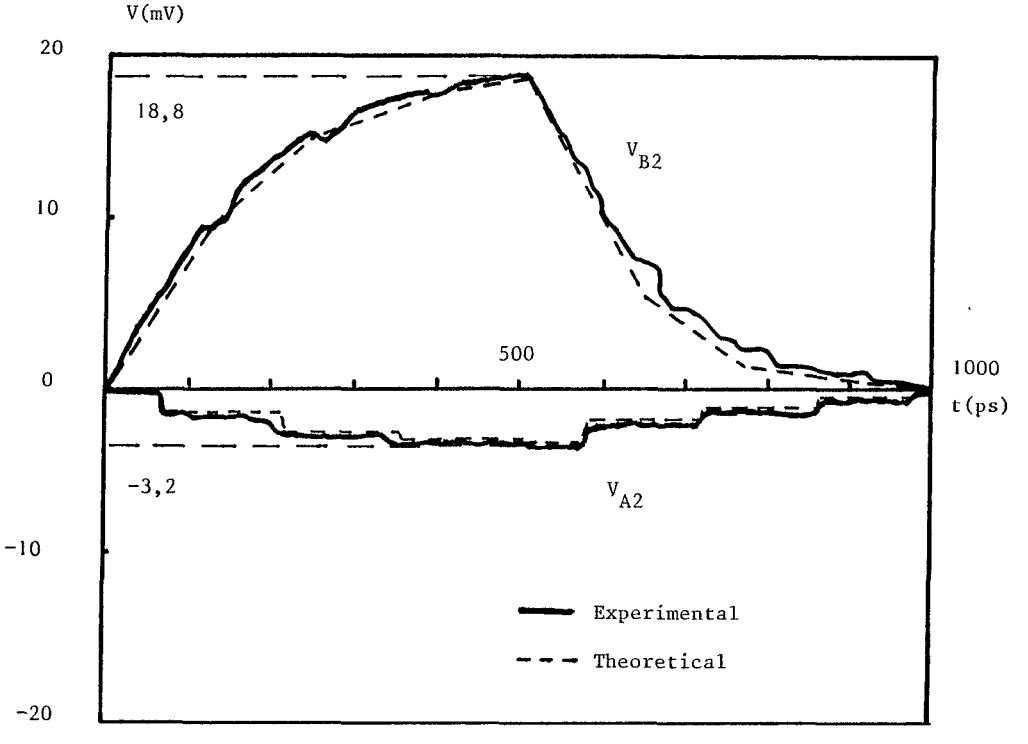


Figure 3

Parasitic voltages induced on signal lines by coupling with power line

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[3] **A.J.Rainal,** "Transmission properties of various styles of printed wiring boards," Bell. Sys. Tech. J., p. 995, Oct. 1978